



## Multibit tribotronic nonvolatile memory based on van der Waals heterostructures

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### ABSTRACT

Low power and multifunctional nonvolatile memories are promising candidates for processing massive data in the Internet of Things era. However, the storage states in conventional memory devices are under the restricted control by electrical or optical signals. Herein, a new multibit tribotronic nonvolatile memory (T-NVM) based on a graphene/hexagonal boron nitride/molybdenum disulfide van der Waals heterostructure and triboelectric nanogenerator (TENG) is proposed. The programming/erasing states can be modulated by the triboelectric potential, which is determined by changing the distance between the two triboelectrification layers. Under the modulation of external mechanical actions, the device exhibits a high on/off ratio of  $10^5$  via manipulating mechanical distance from  $-0.2$  mm to  $+0.2$  mm, a long retention time up to 6000 s, a stable switching behavior for over 100 cycles, and a multilevel data storage capability of 14 stages by different external stimuli. Furthermore, a memory inverter circuit employing the triboelectric potential as input signals can serve as the conversion of logical signals. This work proves the great potential of tribotronic devices for direct interaction with external environment in lower power and broadening diverse applications of human-robot interactions, self-powered wearable devices, and intelligent instrumentation.

### 1. Introduction

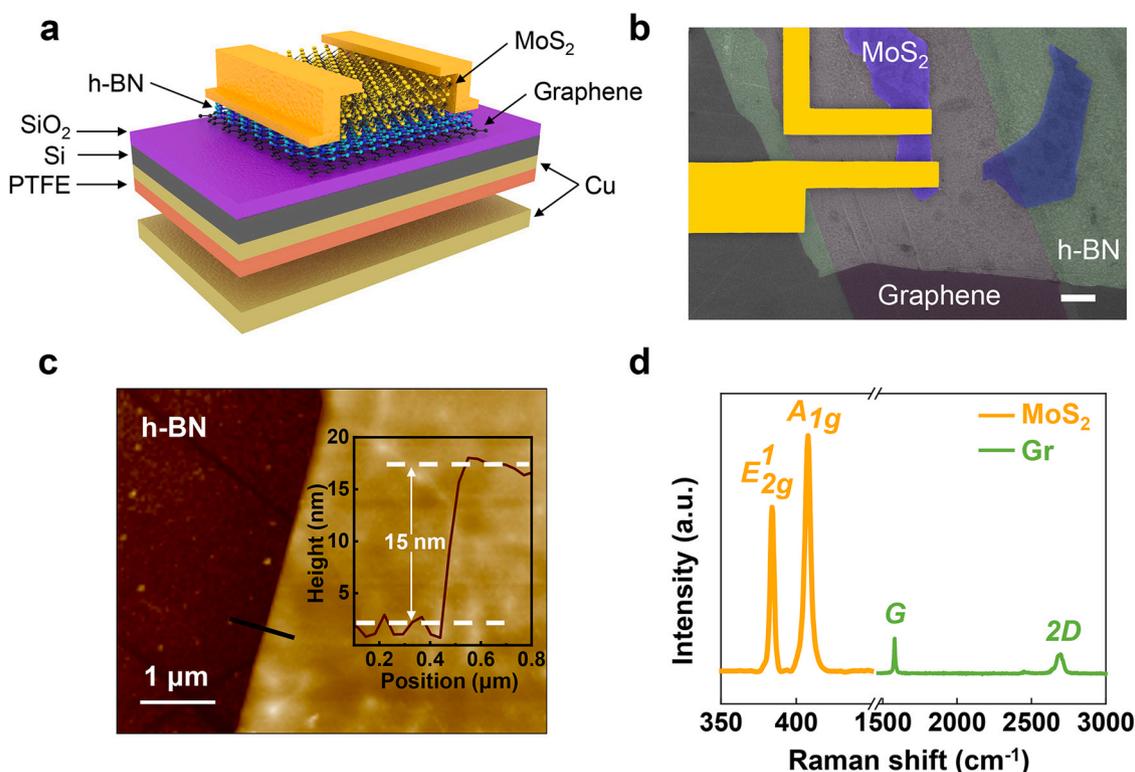
As an essential component in modern information technology, semiconductor memories have always been developed to store massive amounts of data and meet the ever-increasing demands such as high-speed, high-density, long retention time, and low power consumption [1]. Among them, nonvolatile memory (NVM) has been extensively investigated due to high reliability and feasible device fabrication/integration with complementary metal oxide semiconductor techniques [2]. Previous works mainly focus on the innovative memories structure, mechanism, and novel materials with the aim of higher speed, shorter data access time, and further size-scaling. In this context, two-dimensional (2D) materials owning atomic thickness, excellent physical and chemical properties are expected to break through the limitations of feature size scaling and construct sophisticated flexible

and wearable electronic devices in low-cost and lightweight [3–5]. Further, vertically stacked van der Waals heterostructures (vdWHs) based on 2D materials without dangling bonds provide a more promising solution towards multifunctional, superb electronics and optoelectronics. As the isolated atomic layers of 2D materials can be readily recombined to obtain a heterostructure with demanded properties and versatile regulation dimensions [6], the vdWHs have attracted widespread attention on tunneling transistors [7–10], photodetectors [11, 12], nonvolatile memory and logic devices [13,14]. By stacking these van der Waals materials vertically together, the fabricated memories based on vdWHs have achieved the clean interfaces and weak van-der-Waals-like forces between layers. And in the three terminal structure of the source, drain, and gate electrodes, introducing floating-gate layers in vdWHs provides a promising route to guarantee effective data storage and record different stimulus signals by gate

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**Fig. 1.** Structure and morphological characterization of the tribotronic nonvolatile memory. a) Schematic diagram of the memory device based on a graphene/h-BN/MoS<sub>2</sub> heterostructure floating gate transistor and an integrated triboelectric nanogenerator. b) False-colored SEM image of a typical fabricated device. The scale bar is 5  $\mu\text{m}$ . c) AFM image of the exfoliated h-BN flake and the corresponding step-height profile (inset). The height of the flake is 15 nm. d) Raman spectra of the MoS<sub>2</sub> and graphene regions excited by 532 nm laser. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

voltage pulse or light power in previous NVMs [15,16]. Until now, it is still worthy intensive investigation on the stimulus/trigger mode of NVMs because of the limited interaction mechanism between the external environment and memory devices [17–19].

Since 2012, the triboelectric nanogenerator (TEG) based on contact electrification and electrostatic induction has been successfully developed for converting ambient mechanical energy into electricity, which is extensively applied to macro/micro power source [20–23], self-powered active sensors [24,25], and triboelectric-potential driven devices [26–28]. Furthermore, by coupling triboelectricity and semiconductors, an emerging and important field of tribotronics has been established toward triboelectric potential modulation on the charge carrier transport properties. Due to the direct interaction between the external environment and functional electronics, tribotronics have innovative and widespread applications in active tactile sensors [29,30], logic circuits [31], phototransistors [32], organic LED [33], and organic memory [34]. Notably, an organic transistor memory can be programmed and erased effectively by external touch motion and thus achieve a flexible touch monitoring system. Nevertheless, the small programming/erasing current ratio and the short retention time obstruct the further development of multi-level data storage. Another type of tribotronic resistive random access memory, through which the TENG can detect touch signals and the highly integrated system can record signals to realize the function of haptic memory [35]. The low programming/erasing current ratio of this device and the limited resistive switching behavior could not provide distinguishable current states for multilevel data storage. Recently another more type is also used in the touch memory, in which a transistor passivated by an PTFE layer can transduce external touch stimuli to triboelectric charges to modulate the electronic transport in the channel [18]. The small memory window and uncontrollable stored charges hinder its further applications. The required multibit data storage and complexity of process also hinder the low-power-consuming

and practical applications of the tribotronic memory devices. To solve above problems, 2D materials with intrinsically atomic thickness, efficient electrostatic control, superior electrical performance and scaled operating voltage are highly promising to construct functional tribotronic devices for human-machine interaction and low power electronics.

Herein, we demonstrate a new type of multibit tribotronic nonvolatile memory (T-NVM) which integrates a vertically stacked graphene/hexagonal boron nitride (h-BN)/molybdenum disulfide (MoS<sub>2</sub>) van der Waals heterostructure with a contact-separation mode TENG. Unlike traditional nonvolatile memory, the T-NVM can be controlled by mechanical signal, instead of electrical signal. When the friction layer of TENG is approached or separated from the electrode layer under precise control, the corresponding positive/negative inner electrostatic potential will be induced and readily implement the programming/erasing process for the field-effect-transistor nonvolatile memory. The resultant low current level (corresponding to the programming state) and high current level (corresponding to the erasing state) can persist even though the distance is changed back to the initial state. Our T-NVM exhibits a large memory window of about 60 V under electrical control, an on/off current ratio as high as  $10^5$ , a retention time exceeding 6000 s, a good stability after 100 cycles, as well as a multi-level storage capacity of 14 stages by mechanical action stimuli. Moreover, the tribotronic memory logic inverter devices modulated by external action stimuli have also been fabricated and exhibit excellent performance of logic switching. The demonstrated T-NVM and logic circuits based on 2D materials vdWHs with above merits pave the way toward direct interaction mechanism between semiconductor memory devices and external environment, aiming to further broaden the tribotronics in the field of smart electronic devices, and realize active control via human-computer interfacing in intelligent systems.

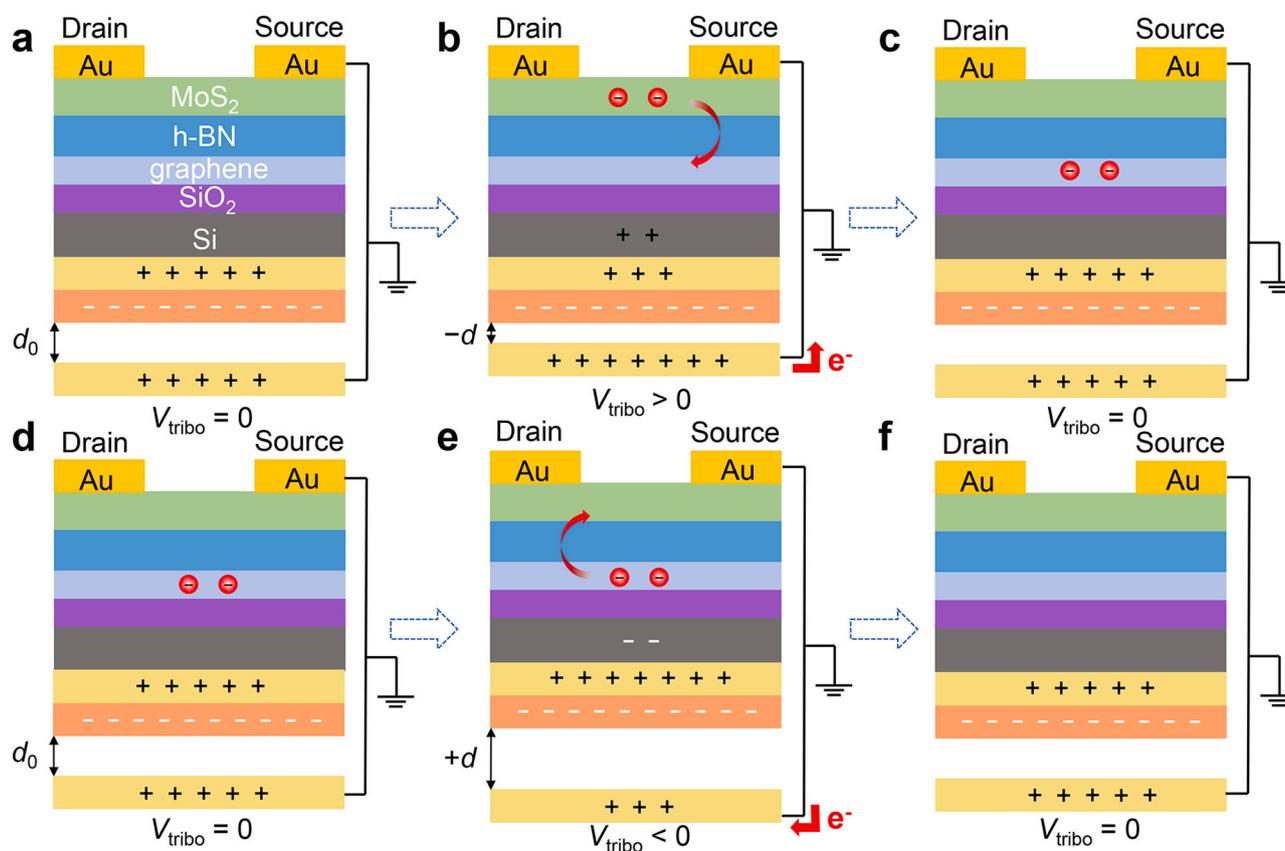


Fig. 2. Schematic illustration of the working principle of the tribotronic nonvolatile memory device. a) The original state with a preset distance ( $d_0$ ) between two frictional layers to get the neutralization state. b) Programming state at a negative relative distance ( $-d$ ) owing to the positive triboelectric potential. c) Off-current reading state after removing changed displacement. d) Programming state without external mechanical motion. e) Erasing state at a positive relative distance ( $+d$ ) owing to the negative triboelectric potential. f) On-current reading state after removing changed displacement.

## 2. Results and discussion

As schematically illustrated in Fig. 1a, our T-NVM is composed of a graphene/h-BN/MoS<sub>2</sub> vdWH and an integrated TENG. The preparation process of the vdWH involves mechanical exfoliation and dry transfer. The complete fabrication process is detailedly described in the Experimental Section and Fig. S1 (Supporting Information). For the graphene/h-BN/MoS<sub>2</sub> vdWH, the top MoS<sub>2</sub> flake acts as the conducting channel, the few-layer graphene transferred on the SiO<sub>2</sub>/Si substrate is used as the potential floating gate, and the h-BN flake (with a large bandgap  $\sim 5.97$  eV) sandwiched between them serves as the proper tunneling barrier. The heavily doped Si and SiO<sub>2</sub> layer work as the control gate and the blocking dielectrics, respectively. The integrated TENG in contact-separation mode comprises of one fixed friction layer (i.e., polytetrafluoroethylene (PTFE) film against the copper (Cu) layer on the back side of Si wafer) and the other mobile friction electrode (i.e., Cu layer attached to a movable acrylic sheet). When the mobile Cu layer is conducted with the periodic contact-separation action against the PTFE friction layer, the triboelectric charges can be induced and coupled to vdWHs transistor through the bottom gate. The vertical distance between PTFE and Cu layer is precisely controlled by a linear position platform and thus the generated triboelectric potential can ensure the effective gating properties and subsequent programming/erasing procedures. Fig. 1b shows a false-color scanning electron microscopy (SEM) image of the fabricated device to present the surface morphology. According to Fig. 1c, the thickness of h-BN flake along the black line was examined to be  $\sim 15$  nm by atomic force microscope (AFM). Before stacking h-BN flake, the Raman spectroscopy of graphene with 532 nm laser excitation is shown in Fig. 1d. The typical G peak at  $1579$  cm<sup>-1</sup> and 2D peak at  $2720$  cm<sup>-1</sup> suggest that the graphene flake is bilayer [36].

The Raman spectrum of MoS<sub>2</sub> exhibits that the in-plane vibration  $E_{1g}$  peak and the out-of-plane vibration  $A_{1g}$  peak locate at  $383.89$  cm<sup>-1</sup> and  $407.76$  cm<sup>-1</sup>, respectively (the wavenumber difference of these peaks is  $\sim 23.87$  cm<sup>-1</sup>), indicating the 3–4 layers nature of the exfoliation-transferred MoS<sub>2</sub> [37,38].

The working mechanism of the tribotronic nonvolatile memory device is schematically illustrated in Fig. 2. Depending on the coupling effects of triboelectrification and electrostatic induction, the triboelectric potential induced by external mechanical motion can take place of the traditional gate voltage and play an essential role in the modulation of the vdWHs floating-gate transistor. In the original state, the Cu and PTFE layers are fully contacted. Due to different electronegativities of the friction layers, electrons are transferred from the mobile Cu layer to the surface of PTFE layer, resulting in the Cu layer being positively charged. The negative electrostatic charges in an equal amount are left on the surface of PTFE film to maintain the electrical neutrality. For the integrated contact-separation mode TENG component, the two friction layers can only be gradually separated in a single direction with the aid of the programmed linear displacement table. Therefore, only negative charges (or positive charges by reverse connecting, i.e. equivalent triboelectric potential in single direction) can be coupled to transistor gate. To solve this problem, we preset the generated triboelectric potential to be 0 V by a short-circuit connection between the top and bottom Cu electrodes after Cu and PTFE are separated at a certain distance of  $d_0$ . Under this circumstance, the induced triboelectric charges are neutralized through the short-circuit connection and there is no voltage drop on the transistor gate. Once there is further decrease or increase of the displacement from the initial distance ( $d_0$ ), the TENG will produce a corresponding positive or negative electrostatic potential to gate the MoS<sub>2</sub> channel. Furthermore, the tunneling-trapped charges by

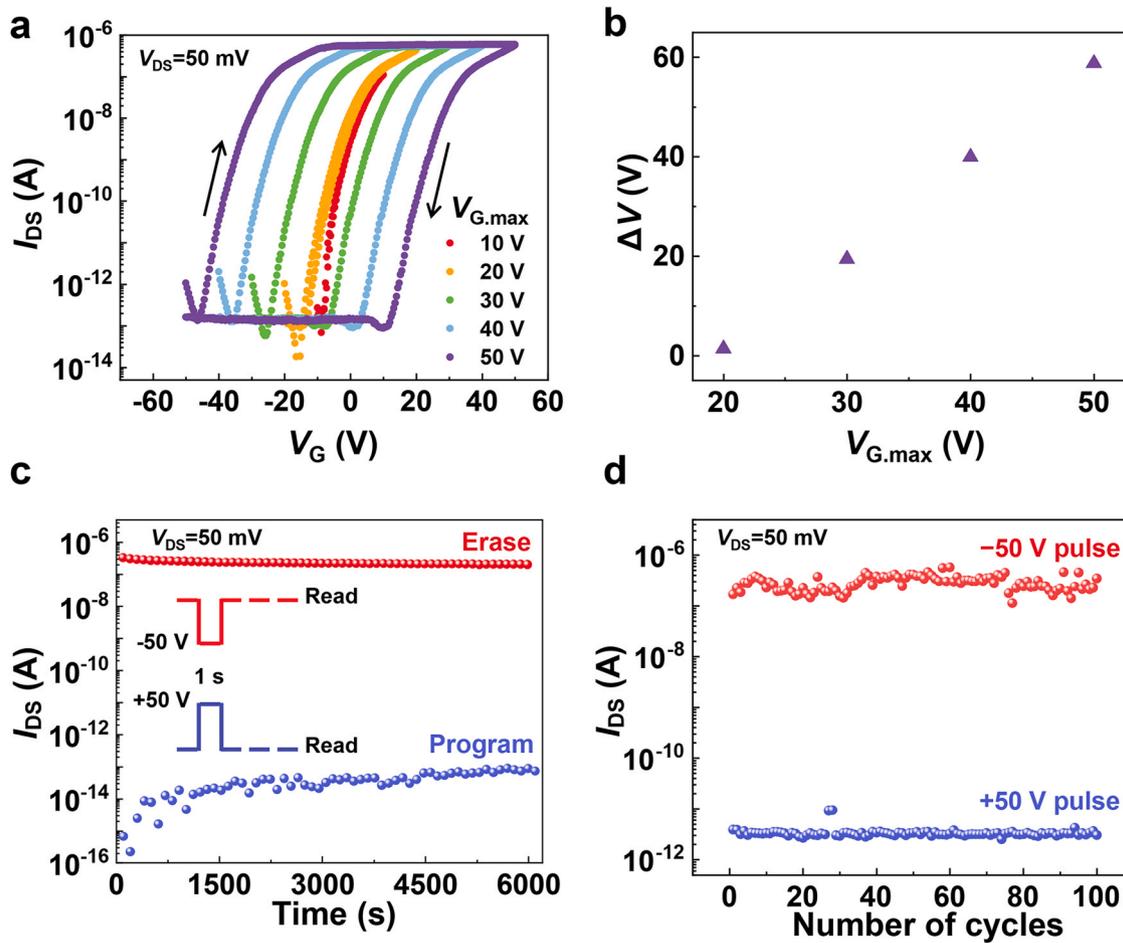


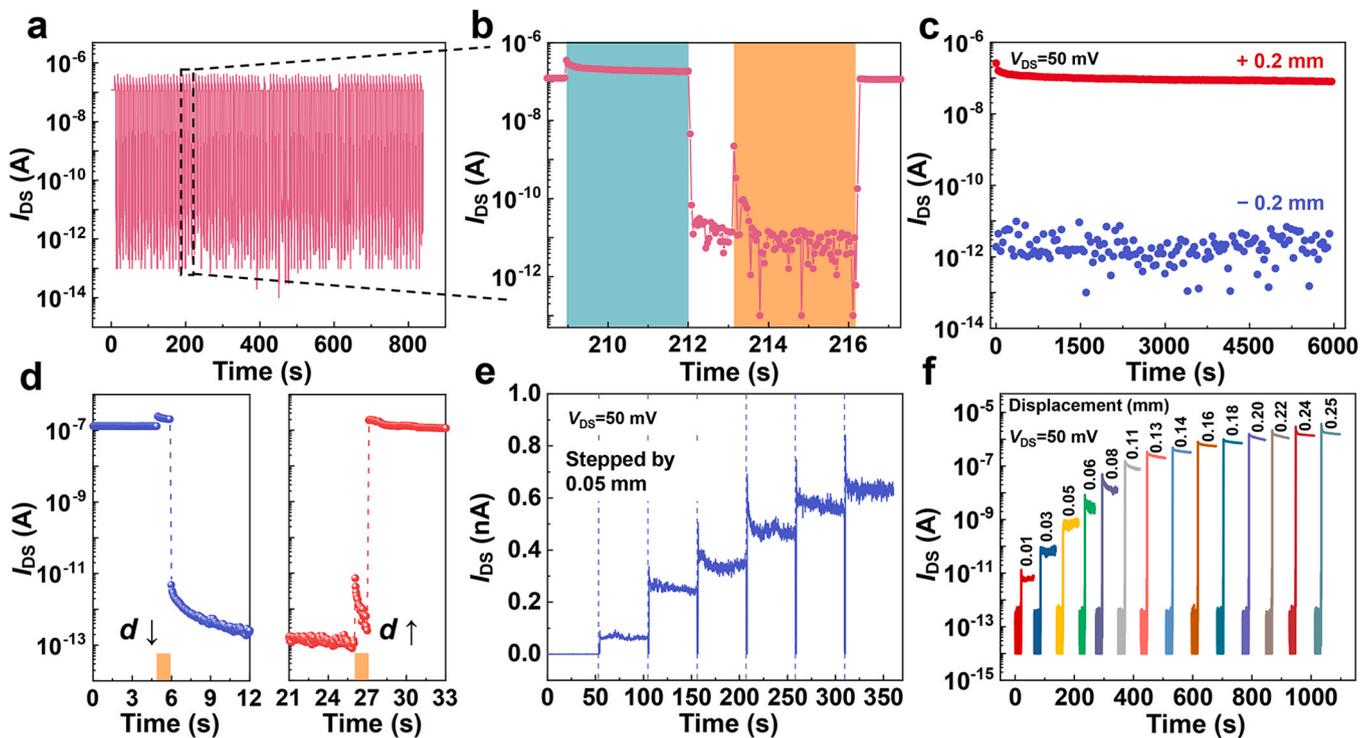
Fig. 3. Characterization of the memory device. a)  $I_{DS}$ - $V_G$  memory hysteresis loops under different control gate voltages at  $V_{DS} = 50$  mV. b) The relationship between the extracted memory window ( $\Delta V$ ) and  $V_{G,max}$  from Figure a. c) Retention properties after applying programming and erasing voltages with 1 s duration under  $V_{DS}$  of 50 mV. d) Endurance performance test for 100 cycles with a  $V_{DS}$  of 50 mV, programming/erasing voltage pulse of +50 V/-50 V and pulse width of 1 s.

graphene layer can be modulated in opposite signs (negative or positive charges) by redefining the initial relative distance ( $d_0$ ). The equivalent triboelectric potential of 0 V at the initial state is critical to make the tribotronic device work in either programming or erasing state by reverse mechanical displacements.

Fig. 2a shows the mechanical programming and erasing procedures for the T-NVM device. An initial relative separation distance ( $d_0$ ) is preset to get the neutralization state with coupled triboelectric gate voltage at 0 ( $V_{tribo} = 0$ ). As the friction distance gradually decreases (Fig. 2b), more positive charges are induced in the mobile Cu layer with electrons flowing to the ground at a negative relative distance ( $-d < d_0$ ). In contrast, the induced triboelectric negative charges in PTFE friction layer lead the left positive charges to flow to the Si gate via the attached Cu electrode, resulting in an equivalent positive gate voltage coupled to the transistor ( $V_{tribo} > 0$ ). At this stage, the positive triboelectric potential will attract the electrons in MoS<sub>2</sub> channel tunneling through the h-BN dielectric (Fowler-Nordheim mechanism) and being trapped by the graphene floating gate (Fig. 2b) [39]. The h-BN dielectrics with an energy barrier can effectively hold the electrons in the floating layer even after removing the positive triboelectric potential pulse. The drain current of the MoS<sub>2</sub> channel can be programmed and maintained at a low-current state because the confined electrons produce a continuous negative electric field to deplete electrons in the MoS<sub>2</sub> channel (Fig. 2c). To implement the erasing process, two friction layers need to separate from each other with induced triboelectric charges gradually vanishing at a positive relative distance ( $+d > d_0$ ). At this stage, electrons will flow back from the ground to the bottom Cu layer, while the induced negative

charges on PTFE will also be neutralized by the positive charges from the attached Cu electrode. The left negative charges are coupled to the vdWH transistor and induce an equivalent negative gate voltage ( $V_{tribo} < 0$ ). The negative  $V_{tribo}$  will drive the electrons trapped in the floating layer back to the MoS<sub>2</sub> channel and implement the erasing state (Fig. 2e). Therefore, the memory transistor can be switched on to the high-current state at the stage as shown in Fig. 2f. In the T-NVM, the basic programming/erasing processes are implemented through external mechanical displacement, which is of great significance to design sophisticated memory devices derived with mechanical behavior. To further understand the detailed physical mechanisms in the electrical and mechanical programming and erasing procedures, corresponding energy band diagrams are illustrated in Fig. S2.

For comparison, the fundamental electrical properties of the memory based on graphene/h-BN/MoS<sub>2</sub> heterostructure were first measured by a probe station in vacuum environment. Fig. 3a displays the typical transfer curves of the nonvolatile memory with a fixed drain voltage of 50 mV, with the gate voltage sweeping from  $\pm 10$  V to  $\pm 50$  V. It's noticeable that different scanning directions, referred to a forward and backward voltage sweep (between -50 V and 50 V), induce a significant shift in the threshold voltage and variable hysteresis window, which is essential electrical behavior for memory devices. The size of memory window ( $\Delta V$ ) is dependent on the scanning range of the  $V_{G,max}$ . A large  $\Delta V$  about 60 V could be obtained with a  $V_G$  sweep range of  $\pm 50$  V. Furthermore, as illustrated in Fig. 3b (the variation of threshold voltage as a function of  $V_{G,max}$ ), the memory hysteresis is also increased with a larger sweeping range of gate voltage. Excellent retention performance

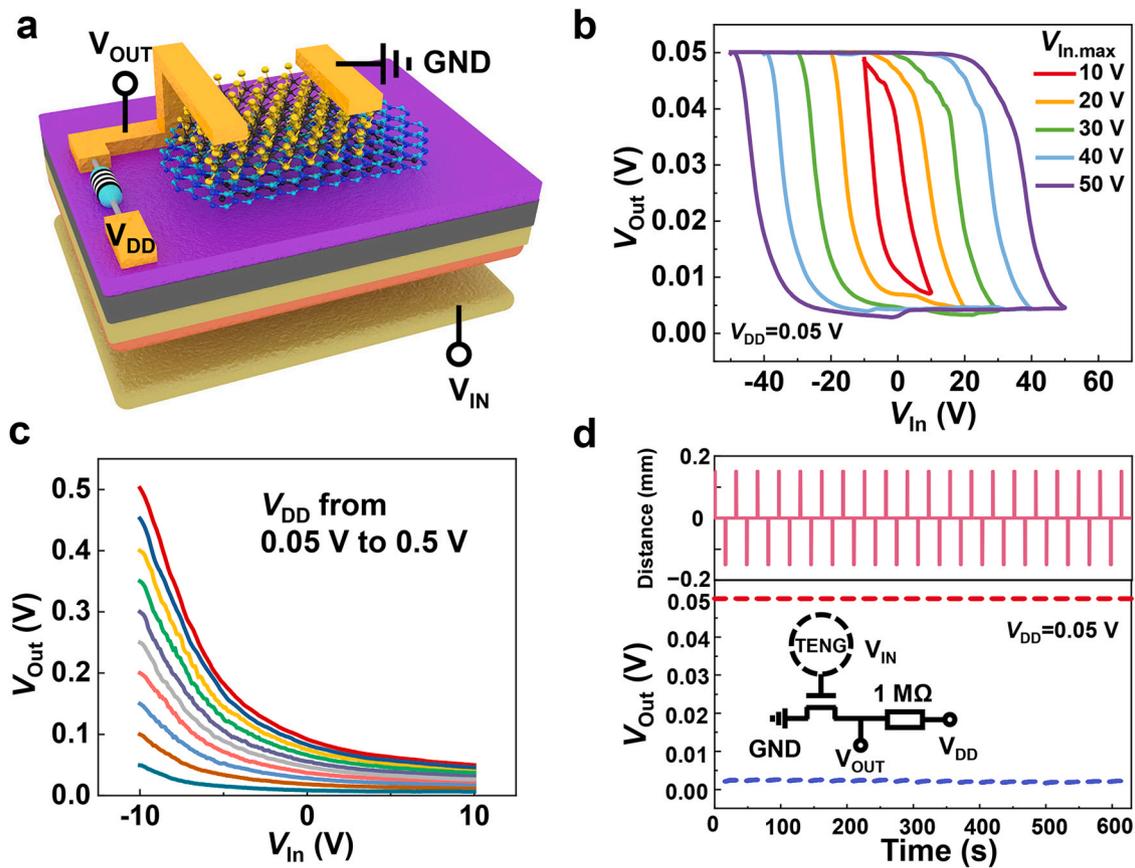


**Fig. 4.** Multiple memory characteristics of the MoS<sub>2</sub>-based tribotronic nonvolatile memory device. a) Endurance test for 100 cycles. Note that the variation of on- and off-current are modulated by the TENG displacement. b) The enlarged view of one cycle in Figure a. Each cycle includes: programming at a negative relative distance (blue region,  $-0.2$  mm, 3 s), erasing at a positive relative distance (orange region,  $+0.2$  mm, 3 s), and reading at  $V_{DS} = 50$  mV for 1 s. c) Retention performance of the memory after applying reverse mechanical displacements ( $V_{DS} = 50$  mV). d)  $I_{DS}$  dynamic response upon the reduced distance ( $d\downarrow$ ) or increased distance ( $d\uparrow$ ) with 1 s duration. e)  $I_{DS}$ -time curve under continuously increasing separation distance between two friction layers with a fixed step distance (0.05 mm), showing the potential of multilevel data storage (7 stages). f)  $I_{DS}$ -time curves under different separation distances from 0.01 mm to 0.25 mm, confirming the capability of multiple memory (14 stages). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

is another critical requirement in memory characteristics. We further evaluated independently the curves of the drain current ( $I_{DS}$ ) over time by applying two opposite  $+50$  V (programming pulse) and  $-50$  V (erasing pulse) for 1 s on the control gate with  $V_{DS}$  fixed at 50 mV. Remarkable electrical properties can be observed in Fig. 3c that the current ratio of erasing/programming state is determined to exceed  $10^6$  and the memory device can maintain long-term stability for more than 6000 s with only a minor change of the current. The good retention time is attributed to that the tunneling layer with controlled moderate thickness can help electrons to store in the graphene floating layer for prolonged time. To further measure the dynamic response characteristics of the memory devices, the dynamic programming/erasing cycle test was conducted with  $V_{DS} = 50$  mV (Fig. 3d). The memory was initially set as the programming state (OFF state) with the application of  $V_G (+50$  V) pulse for 1 s and the  $I_{DS}$  considerably decreases to  $3 \times 10^{-12}$  A immediately. After resetting  $V_G$  to 0 V, the  $I_{DS}$  was still in a low current state. While applying a  $V_G$  pulse of  $-50$  V for 1 s, the memory was instantly switched to the erasing state (ON state), reaching  $3 \times 10^{-7}$  A, and it can retain the high current state after removing the gate voltage. In the whole program-read-erase-read cycles (100 cycles), the response of the device is very stable in all the gating stages.

To illustrate sufficiently the work principle of tribotronic nonvolatile memory devices and make a clear comparison with the electrical properties by applying voltage, we conduct the measurement on the memory electrical behaviors by applying mechanical displacement of the integrated TENG component. To precisely control the applied equivalent gate voltage (i.e., triboelectric potential), we use an electrometer (Keithley 6514) to monitor the TENG output simultaneously during the test. The integrated TENG component working in a contact-separation mode provides different voltages by changing the separation distance between two friction layers. Such voltages can be utilized

to directly and effectively drive and program the memory devices. The output voltage of TENG under separation-contact-separation process with a periodic step of 0.05 mm is monitored to be very stable as shown in Fig. S3a. Accordingly, the durability characteristic of the T-NVM is still remarkable as presented in Fig. 4a. With the relative distance changing from  $-0.2$  mm (programming) to 0 mm (reading) and from  $+0.2$  mm (erasing) to 0 mm (reading) and a bias voltage of 50 mV, one complete programming/erasing (P/E) cycle is finished. Corresponding output voltage of the driving-TENG related with the displacement between PTFE and Cu layers can be found in more details in Fig. S3b and the instantaneous output voltage of TENG can reach approximately  $\pm 50$  V (Fig. S3c). In the endurance characteristic, the T-NVM modulated by TENG mechanical displacement has the same stable dynamic response after 100 cycles. Fig. 4b details one complete cycle including the TENG-driven programming process (blue area, 3 s)- off state reading (1 s)- erasing process (orange area, 3 s)- on state reading (1 s). A large on/off current ratio of about  $10^5$  was obtained in Fig. 4c. Compared to Fig. 3c ( $I_{on/off} \approx 10^6$ ), a reduction in the magnitude of the erasing/programming current ratio is possibly coming from the different vacuum status of the measurement environment. By further shortening the duration time of displacement to 1 s, we obtained the dynamic response of the  $I_{DS}$  upon the reduced distance or increased distance (Fig. 4d). Moreover, the achieved high P/E current ratio is a prerequisite to practical multibit (or multilevel) data storage applications. Different current retention levels can be realized by applying stepped multiple displacement changes or applying various stimuli at different distances. As shown in Fig. 4e, the memory was first programmed by the mechanical displacement for 1 s. With gradually increased separation distance (stepped by 0.05 mm), the corresponding triboelectric potential pulse can gradually attract more and more electrons tunneling to the graphene layer, resulting in seven continuously increased current stages.



**Fig. 5.** Structure schematic and electrical characteristics of the resistive-load inverter circuit. a) 3D view of the nonvolatile memory inverter logic circuit with a  $R_{\text{ext}}$  (1 M $\Omega$ ) as the load. b) Typical  $V_{\text{Out}}-V_{\text{In}}$  transfer curves with various input voltage scanning ranges at a  $V_{\text{DD}}$  of 0.05 V. c) Output characteristics of the inverter under  $V_{\text{DD}} = 0.05-0.5$  V stepped by 0.05 V. d) Switching behavior between on- and off-current states at  $V_{\text{DD}} = 0.05$  V. The input port is modulated with TENG relative displacement and the curves correspond to the off state (applying  $-0.15$  mm relative distance, 1 s) and on state (applying  $+0.15$  mm relative distance, 1 s). Inset figure presents the simplified circuit diagram.

Fig. 4f shows the distinct  $I_{\text{DS}}$  curves during the off-current and different mechanical displacements, and the memory was first programmed at the same off-current level. By changing the distance stepwise from 0.01 mm to 0.25 mm ( $V_{\text{DS}} = 50$  mV),  $I_{\text{DS}}$  showed a clearly distinguishable increment with 14 current levels from  $10^{-11}$  A to  $10^{-6}$  A with increasing vertical separation distance (corresponding to different equivalent gate voltages). This method proves another feasibility of implementing multibit storage, which is different from applying displacement repeatedly. Overall, the achieved results indicate that the triboelectric potential works efficiently on nonvolatile memories similar to the applied electrical gate voltage. A tiny movement of the friction layer can realize a successful dynamic modulation with good stability, reliability and multilevel tribotronic data storage, encouraging a broader range of applications in human-machine interaction. Meanwhile, the memory device can be modulated by external mechanical motion rather than persistent light illumination or high gate voltage, which is of significance for the low power consumption.

To make better use of the superior performance of the T-NVM and extend more advanced applications, the developed T-NVM can be exploited in logic inverter circuits as well. The logic memory circuits are implemented by connecting the memory device to a large external load resistor ( $R_{\text{ext}}$ , 1 M $\Omega$ ) in series with a supply voltage ( $V_{\text{DD}}$ ) applying to the drain electrode (Fig. 5a). In this configuration, the input voltage is provided by the well-controlled displacement of the TENG, similar with the T-NVM test. Fig. 5b shows the typical voltage transfer curves (output voltage ( $V_{\text{Out}}$ ) vs input voltage ( $V_{\text{In}}$ )) upon various sweeping input voltage ranging from  $\pm 10$  V to  $\pm 50$  V with a fixed  $V_{\text{DD}}$  of 50 mV. The large hysteresis matches well with the curves in Fig. 3a. However, the

voltage signal is significantly different in the programming/erasing states. As shown in Fig. 5c, under a various  $V_{\text{DD}}$  of 0.05–0.5 V, the  $V_{\text{Out}}$  decreases as the  $V_{\text{In}}$  increases. As the voltage dropping over the external resistance varies with the resistance change of the memory device, a logical 1 (high  $V_{\text{Out}}$ , about 0.05 V) is acquired at  $V_{\text{In}}$  of  $-10$  V (low  $V_{\text{In}}$ , a logical 0) at  $V_{\text{DD}} = 0.05$  V, demonstrating the NVM is capable of switching signals as a logic inverter. The dynamic switching behavior of the circuit is also investigated and the inset of Fig. 5d shows the equivalent electrical circuit diagram of the T-NVM based on the contact-separation TENG component. It's noticed that when a positive displacement ( $+0.15$  mm) is applied, the achieved  $V_{\text{Out}}$  (high  $V_{\text{Out}}$ , about 0.05 V) is approximately equal to the  $V_{\text{DD}}$  (a logical 1). In contrast, a negative displacement ( $-0.15$  mm) can rapidly switch the circuit to the off state, causing a logical 0 (low  $V_{\text{Out}}$ , about 0 V). The dynamic switching behavior can achieve good repetition for 20 cycles during periodic displacement, exhibiting a stable and repeatable gating modulation by TENG. In this way, our tribotronic memory inverter circuits can realize repeatable and low-power logical signal conversion by simply applying the external mechanical motion, which broadens the application field for smart electronic devices.

### 3. Experimental section

#### 3.1. Device fabrication

Few-layer graphene, h-BN and MoS<sub>2</sub> flakes were all obtained by mechanical exfoliation process. First, the few-layer graphene flake was directly exfoliated on a Si/SiO<sub>2</sub> (285 nm SiO<sub>2</sub>) substrate. Subsequently, h-BN flakes (with thickness about 15 nm) were

produced onto the polydimethylsiloxane (PDMS) stamp by 3 M scotch tape and placed onto the graphene flake with the help of an optical microscope (OM). After that, the MoS<sub>2</sub> flake was aligned on the graphene/h-BN stack by a similar dry transfer method (see [Supplementary Fig. S1](#)) [40]. Source and drain electrodes were patterned by electron beam lithography and then Cr/Au (10/50 nm) electrodes were deposited by e-beam evaporation. The NVM was coupled with a TENG as the T-NVM.

### 3.2. Device characterization

The morphology of fabricated devices was obtained by OM and SEM (Nova NanoSEM 450), and the thickness of few-layer flakes was characterized by AFM and Raman spectroscopy. Electrical properties of NVM devices were measured using a Keithley 4200 semiconductor parameter analyzer at room temperature (in vacuum environment). The subsequent electrical measurements of T-NVM were carried out with a semiconductor characterization analyzer (Agilent B1500A) in the ambient environment. When the TENG was controlled by a linear motor, the output voltages were recorded simultaneously with a Keithley 6514 system electrometer.

## 4. Conclusion

In summary, a multibit tribotronic nonvolatile memory is designed and fabricated by using a graphene/h-BN/MoS<sub>2</sub> van der Waals heterostructure and a contact-separation mode TENG. Different from traditional programming/erasing electrically and optically like most other memory devices, the properties of our device are modulated just by changing the mechanical displacement between two friction layers. Under the synergistic effect of the floating gate, the electrons in the MoS<sub>2</sub> channel can tunnel to the graphene and be stored in or released from the floating gate through the generated positive and negative electrostatic potential as an external gate voltage alternative, thereby enabling the programming/erasing states. Besides a large memory window of 60 V, the T-NVM exhibits a high on/off current ratio of  $\approx 10^5$ , a long retention time for up to 6000 s, and multiple P/E cycles progress under the action of short displacement which are comparable to the performances of electrical control. On the basis of triboelectric-charges control, the memory can be further erased by changing the displacement multiple times to achieve seven stages and controlling the different separation distances to obtain 14 current stages. Furthermore, the application of triboelectric potential as input voltage makes our memory coupled with a TENG can be extended to a logic inverter circuit successfully. Together, all performances mentioned demonstrate that the tribotronic nonvolatile memory and subsequent inverter circuits are allowed active interaction by integrating with external mechanical motion, providing a versatile and multifunctional platform for the application of tribotronics in multilevel data storage, human-machine interaction, and intelligent systems.

### CRedit authorship contribution statement

**Mengmeng Jia:** Writing - original draft, Writing - review & editing, Investigation, Formal analysis, Methodology. **Jinran Yu:** Writing - review & editing, Methodology. **Yudong Liu:** Validation. **Pengwen Guo:** Methodology. **Ying Lei:** Formal analysis. **Wei Wang:** Formal analysis. **Aifang Yu:** Conceptualization. **Yaxing Zhu:** Investigation. **Qijun Sun** and **Junyi Zhai:** Supervision, Project administration, Funding acquisition, Writing - review & editing. **Zhong Lin Wang:** Supervision, Project administration.

### Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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## Appendix A. Supporting information

Supplementary data associated with this article can be found in the online version at [doi:10.1016/j.nanoen.2021.105785](https://doi.org/10.1016/j.nanoen.2021.105785).

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